Advanced Analog Integrated Circuits

Matching

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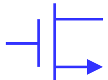
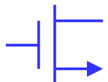
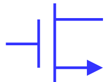


Issue

- In SPICE, two transistors with equal dimensions and terminal voltages (and temperature) carry the same current
- In Si, the current are (slightly) mismatched
  - Why?
  - How much mismatch?
  - Fix?
  - Verification?



Origins of Mismatch



Wafer to Wafer Variations

Wafer 1

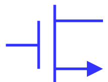
- all NMOS fast
- all PMOS nominal
- all C nominal
- all R fast

Wafer 2

- all NMOS slow
- all PMOS slow
- all C fast
- all R nominal

Parameter	Slow	Nominal	Fast
V_{TH}	0.5V	0.4V	0.3V
μC_{ox} (NMOS)	200 $\mu A/V^2$	250 $\mu A/V^2$	300 $\mu A/V^2$
μC_{ox} (PMOS)	100 $\mu A/V^2$	130 $\mu A/V^2$	160 $\mu A/V^2$
C_{MIM}	1.2 $fF/\mu m^2$	1 $fF/\mu m^2$	0.8 $fF/\mu m^2$
R_{poly}	80 $\Omega/\square$	70 $\Omega/\square$	60 $\Omega/\square$
R_{nwell}	1.3 $k\Omega/\square$	1 $k\Omega/\square$	0.7 $k\Omega/\square$

- Verify performance for all combination (with simulator)
- Also low/high supply and temperature



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Random Variations

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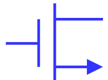
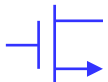


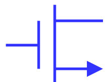
Random Variations

Ref: M. Pelgrom, "Matching properties of MOS transistors," IEEE JSSC, 10/1989, pp. 1433-9.

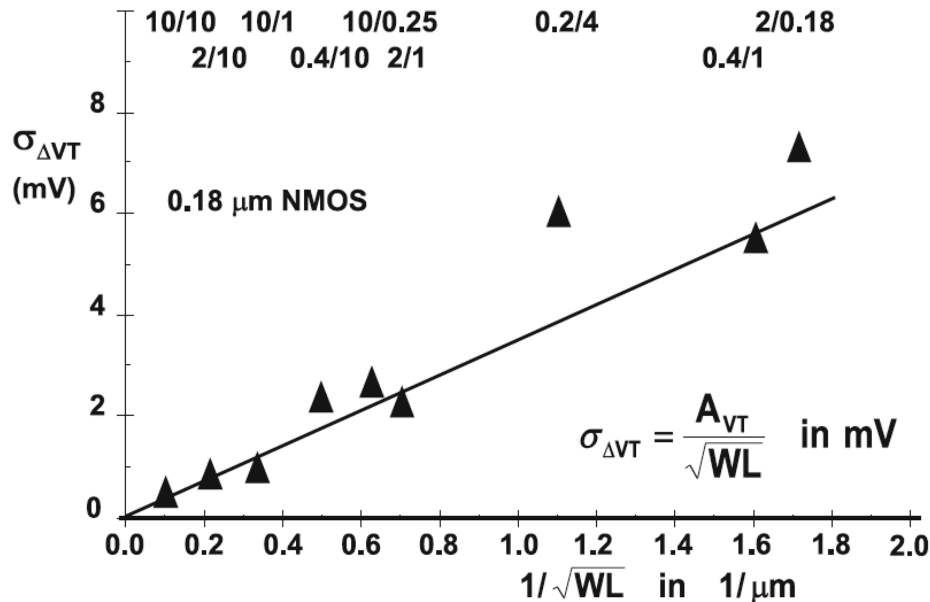


Parameters for typical 180nm CMOS

Parameter	Value
A_{vt} (MOS)	5 mV-µm
A_{β} (MOS)	1 %-µm
$A_{\Delta Is/Is}$ (BJT)	2 %-µm
$A_{\Delta\beta/\beta}$ (BJT)	4 %-µm
$A_{\Delta C/C}$ (MIM capacitor)	1 %-µm
$A_{\Delta R/R}$ (Poly resistor)	3 %-µm

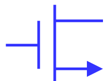


A_{vt} for 180nm CMOS

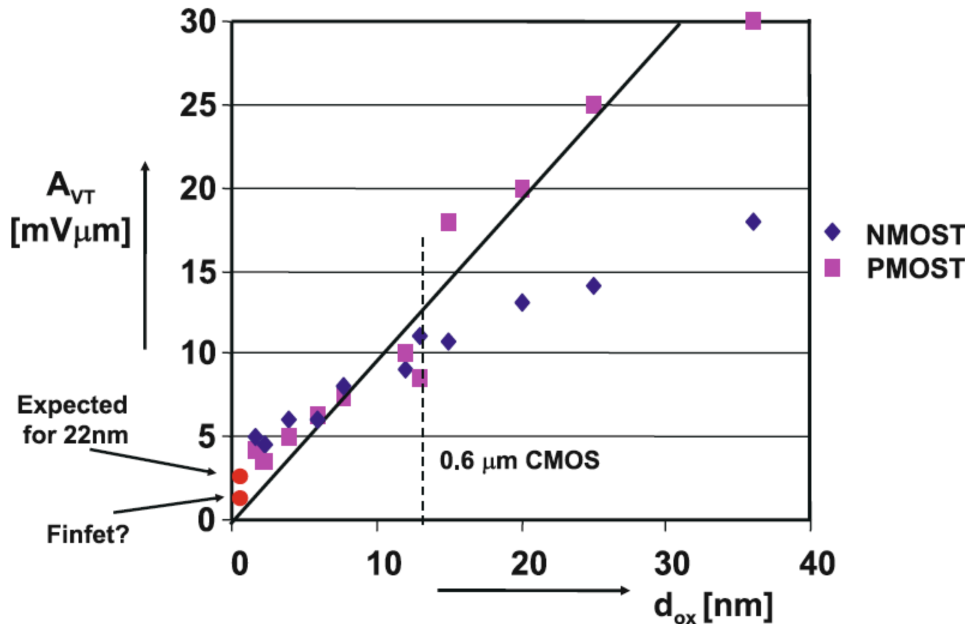


Ref: M. Pelgrom et al, "A designer's view on mismatch," Chapter 13 in Nyquist A/D Converters, Sensors, and Robustness, Springer 2012, pp. 245-67.

- Good match between heuristic model and experimental data, except
  - minimum channel length (actual length is smaller than drawn)
  - very long channel device

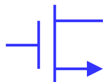


A_{vt} versus Gate Oxide Thickness



Ref: M. Pelgrom et al, "A designer's view on mismatch," Chapter 13 in Nyquist A/D Converters, Sensors, and Robustness, Springer 2012, pp. 245-67.

- A_{vt} increases $\sim 1\ \mathrm{mV} \times \mu\mathrm{m}$ for every nm of gate insulator thickness
  - for well-engineered process
- But: circuits get smaller …
- A_{vt} scaling design: e.g.
  - Outlier for 0.6μm PMOS is result of compensating implant, leading to high variability
  - beyond 0.6μm node dedicated well implant is used



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Yield

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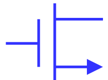
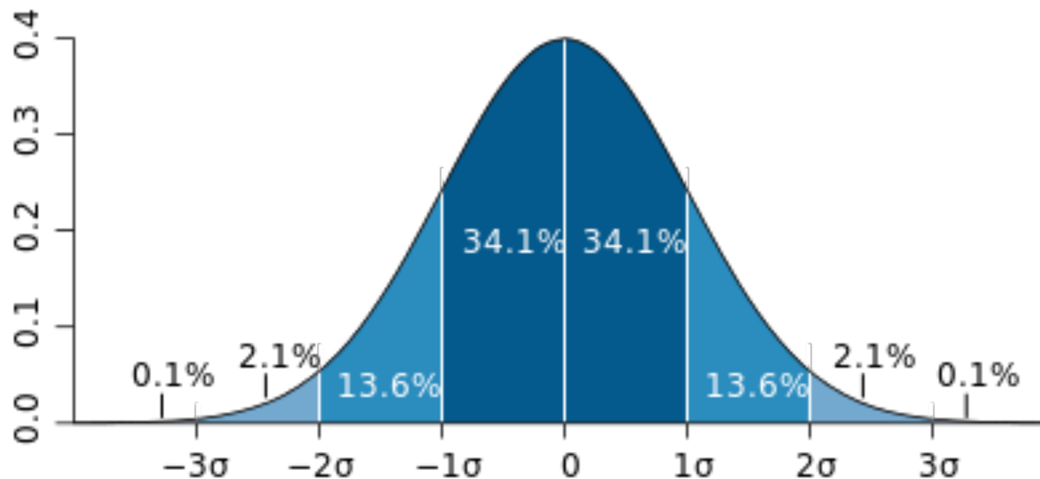


Random Mismatch - Example

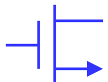
What is the mismatch between two MIM capacitors with $W = L = 20\mu\text{m}$?

$$\sigma_{\Delta C/C} = \frac{A_{\Delta C/C}}{\sqrt{20\mu\text{m} \times 20\mu\text{m}}} = \frac{1\% \times \mu\text{m}}{20\mu\text{m}} = 0.05\%$$

→ 68.2% of all devices fabricated match to ±0.05%.



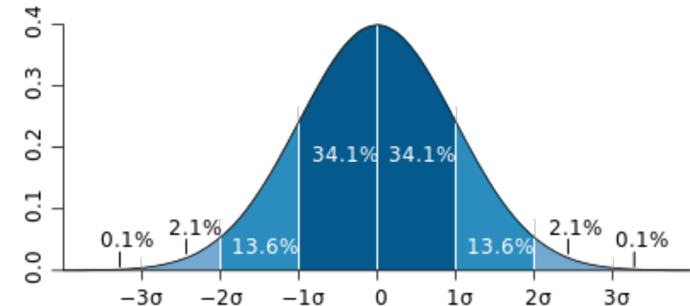
https://en.wikipedia.org/wiki/Standard_deviation



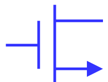
Yield

- Fraction of devices that meet specification

Interval	Yield	Fraction Bad
1σ	68.3%	1/3
2σ	95.4%	1/22
3σ	99.7%	1/370
4σ	99.99%	1/16,000
5σ	99.999%	1/1,700,000
6σ	99.999 999 8%	1/507,000,000



- Large customers tolerate less than 1ppm failures
  - 6σ design
  - Testing, binning
  - Capacitor example: 1σ → ±0.05%, 6σ → ±0.3%,



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Mismatch in Mirrors and Differential Pairs

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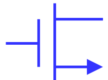
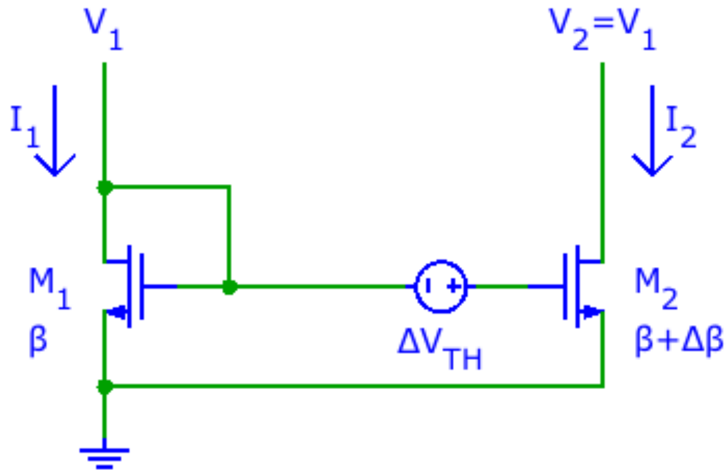
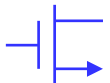
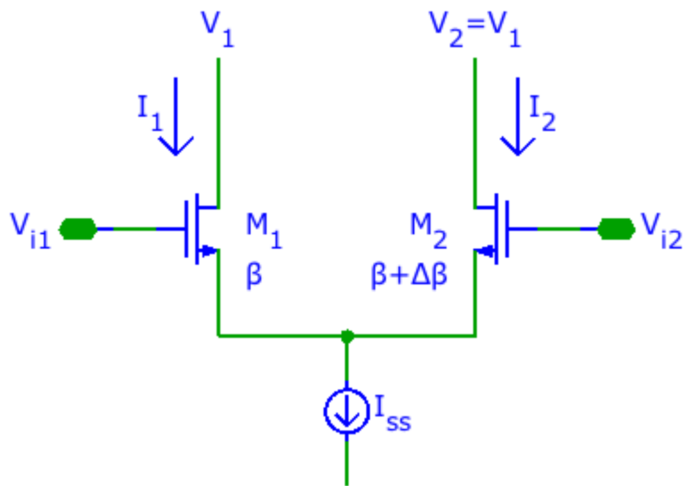


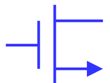
Mismatch in Current Mirror





Differential Pair

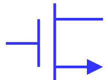




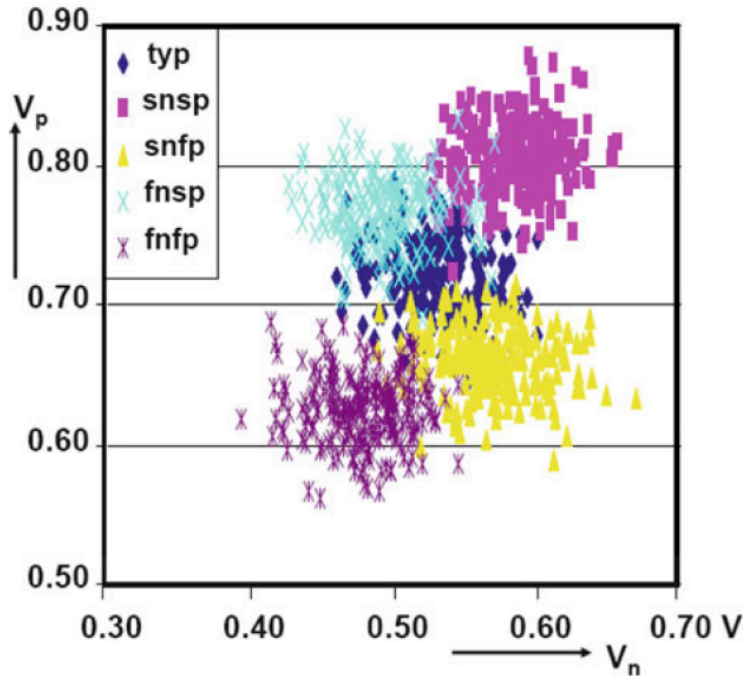
Verification

1. PVT
   – Process, voltage, temperature
   – Perform verification for all combinations on design and extracted netlist

2. Random variations
   – Monte-Carlo analysis



Technology Trend



- slow/fast spread decreases
  - better process control
- random variations increase
  - smaller devices

V_{TH} spread for 90nm NMOS and PMOS:

➢ random variations comparable to slow/fast spread

Ref: M. Pelgrom et al, “A designer’s view on mismatch,” Chapter 13 in Nyquist A/D Converters, Sensors, and Robustness, Springer 2012, pp. 245-67.